REMARKS

The original patent included five claims. Claims 6-16 were added in the reissue application. Claims 6-12 are amended in this paper, and claims 1-16 remain pending for examination. Reexamination of claims 1-16 is therefore respectfully requested.

Claims 1-16 were pending for examination in the last office action. These claims were rejected under 35 U.S.C. § 251 as being based upon a defective reissue oath as being related to a subject matter of a canceled non-elected claim in the original patent. This rejection is based on the "recapture" doctrine, which forbids claims "that are broader than the original patent claims in a manner directly pertinent to the subject matter surrendered during prosecution." 1/

The application that led to the original patent included eight claims. Claims 1-5 were directed to a probe card, 6 and 7 to a probing test system, and claim 8 to a probing test method. These claims were subject to a restriction requirement, in response to which the Applicant elected claims 1-5 for prosecution in the original application. Claims 6-8 – including method claim 8 – were canceled. Claims 1-5 were examined and ultimately issued in the patent.

New claims 6-16 are method claims. The Examiner objects to the presentation of these claims in the reissue application in view of the cancellation of method claim 8 from the original application. This, though, is an overbroad application of the recapture doctrine.

It is true that the recapture doctrine can arise when subject matter is surrendered during the original patent's prosecution. 2/ This can happen when

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1/ *Hester Indus., Inc. v. Stein, Inc.*, 142 F.3d 1472, 1480 (Fed. Cir. 1998).

2/ *See generally, Hester v. Stein*, at 1480-81.

broad claims are cancelled or narrowed, [3] or even, in some cases, through prosecution arguments alone. [4]

The recapture doctrine has its limits, though. Significantly, the recapture doctrine does not apply where the alleged "surrender" is not fairly "an admission that the scope of [the original] claim was not in fact patentable." [5]

The recapture doctrine is limited, moreover, to cases in which the applicant seeks new claims that are *as broad or broader than the claims that were surrendered.* The recapture doctrine bars claims "that are of the *same* or of *broader scope* than those claims that were canceled from the original application." [6] "In contrast, a reissue claim narrower in scope escapes the recapture rule entirely." [7]

In this case, the recapture doctrine does not apply because the Applicant's withdrawal of original method claim 8 in response to the restriction requirement cannot be viewed as "an admission that the scope of [original claim 8] was not in fact patentable." [8] The new claims, moreover, are all *narrower* than the original method claim – and thus not subject to the recapture doctrine for this reason as well.

A restriction requirement says nothing about the ultimate patentability of any of the claim to which it applies. No reference is made to prior art or even to the form of the claims. Restriction is in this respect purely procedural. Restriction is merely an allegation by the Office that multiple inventions are present in a single

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[3] *Id.*

[4] *Id.* at 1481.

[5] *Seattle Box Co. v. Industrial Crating & Packing, Inc.*, 731 F.2d 818, 826 (Fed. Cir. 1984), *see also, In re Clement*, 131 F.3d 1464, 1468 (Fed. Cir. 1997); and *Mentor Corp. v. Colorplast, Inc.*, 998 F.2d 992, 995 (Fed. Cir. 1993), *all cited in Hester v. Stein*, 142 F.3d at 1472.

[6] *Ball Corp. v. United States*, 729 F.2d 1429 (Fed. Cir. 1984)(original emphasis).

[7] *In re Clement*, 131 F.3d 1464, 1469 (Fed. Cir. 1997).

[8] *See, Seattle v. Industrial Crating*, 731 F.2d at 826.

application. 9/ An applicant's acquiescence to this allegation is not in any way an admission that the withdrawn claims are not patentable, and the withdrawal of original claim 8 from the original application in this case is thus no proper basis for application of the recapture doctrine.

Cancellation of a non-elected claim in response to a restriction requirement is clearly not an admission that the claim is not patentable. To the contrary, applicants routinely resubmit such claims in divisional applications. If the applicant had chosen to do so here, he would have been entirely free to resubmit non-elected method claim 8 in his own divisional application. The applicant did not chose to do so, and had applicant re-submitted a claim identical or substantially equivalent to original method claim 8, the Examiner might legitimately have rejected that claim as being based on an ineligible and uncorrectable error. 10/

That is not the type of error the applicant seeks to correct in this reissue application. As the reissue declaration states:

> The claims of U.S. Patent No. 5,818,249 are defined in terms of signal lines carrying both a test signal and a response signal. This is unduly restrictive in that aspects of the invention can be practiced using other test methodologies. The newly presented claims do not include this error.

New claims 6 and 16 omit the elements of the issued claims that require signal lines carrying both a test signal and a response signal. New claims 6 -16 are broader than the issued claims in this respect. New claims 6-16 are also method claims, and broader for this reason as well. That new claims 6-16 are method claims does not by itself bar their presentation in a reissue application. Applicant's counsel is unaware of any authority that says that the withdrawal of a method

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9/ *See, generally, Manual of Patent Examining Procedure* §§ 801 *et seq.*

10/ *See, M.P.E.P.* § 1402 ("A reissue applicant's failure to timely file a divisional application is not considered to be error causing a patent granted on elected claims to be partially inoperative by reason of claiming less than the applicant had a right to claim.")

claim from an application in response to a restriction requirement forever bars the presentation of any other method claim in a subsequent reissue application.

The recapture doctrine is further inapplicable to the new claims, moreover, because new claims 6-16 are *narrower* than the original claim that was allegedly surrendered.[11] The original method claim 8 and the first independent reissue claim 6 are presented below side-by-side for comparison:

Withdrawn Application Claim 8:	Reissue Claim 6 (Before Amendment):
A probing test method for testing semiconductor integrated circuits arranged on a semiconductor wafer in rows and columns, comprising the steps of:	A method of manufacturing integrated circuit chips, comprising:
setting probe needles into contact with pads of semiconductor integrated circuits arranged in at least two columns; and	providing a semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged theron in two columns and at least two rows, each of said plurality of semiconductor integrated chips having a plurality of external terminals;
	coupling a probe card to the semiconductor wafer through a plurality of probe needles on said probe card corresponding to said plurality of external terminals of each of said integrated circuit chips, said probe card receiving a plurality of independent test signals and a power supply signal from a tester;
simultaneously testing the semiconductor integrated circuits arranged in at least two columns to determine electrical characteristics of the semiconductor integrated circuits.	concurrently supplying the independent test signals and the power supply signal from the tester through the probe needles to said plurality of external terminals of said plurality of integrated circuits; and

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[11]/ *In re Clement*, 131 F.3d 1464, 1469 (Fed. Cir. 1997). Note that the appropriate comparison is the reissue claim against the claim *withdrawn from the original application*. It is immaterial whether the reissue claim might be broader in some respects than the claims *issued in the patent*, as is the case here, and as is frequently the case in reissue applications filed before the two-year deadline.

concurrently measuring electric characteristics of said semiconductor integrated circuit chips in an independent manner.

Claim 6 of the reissue application is narrower in several respects in comparison with claim 8 that was withdrawn from the original application. The original withdrawn claim would have required simply:

> setting probe needles into contact with pads of semiconductor integrated circuits arranged in at least two columns.

The newly-presented reissue claim is much more specific, requiring:

> providing a semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged theron [*sic*, thereon] in two columns and at least two rows, each of said plurality of semiconductor integrated chips having a plurality of external terminals; [and]
>
> coupling a probe card to the semiconductor wafer through a plurality of probe needles on said probe card corresponding to said plurality of external terminals of each of said integrated circuit chips, said probe card receiving a plurality of independent test signals and a power supply signal from a tester.

As for testing the circuits, withdrawn claim 8 would have required only:

> simultaneously testing the semiconductor integrated circuits arranged in at least two columns to determine electrical characteristics of the semiconductor integrated circuits.

Again, newly presented claim 6 is considerably more specific in requiring:

> concurrently supplying the independent test signals and the power supply signal from the tester through the probe needles to said plurality of external terminals of said plurality of integrated circuits; and
>
> concurrently measuring electric characteristics of said semiconductor integrated circuit chips in an independent manner.

Reissue claim 8, as amended in this paper, is narrower still, as are reissue claims 9-11, which depend from it. The recapture doctrine thus does not apply to these claims, because they are narrower in all material respects than the claim cancelled from the original application.

The same is true of reissue claims 12-16. The original claim 8 and the second independent reissue claim (claim 12) are set out below, again side-by-side for comparison.

Withdrawn Application Claim 8:	Reissue claim 12 (Before Amendment):
A probing test method for testing semiconductor integrated circuits arranged on a semiconductor wafer in rows and columns, comprising the steps of:	A probing test method of semiconductor integrated circuits, comprising:
setting probe needles into contact with pads of semiconductor integrated circuits arranged in at least two columns; and	preparing at least one semiconductor wafer, said semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in rows and columns, said semiconductor integrated circuit chips having a plurality of external pads; preparing at least one probe card, said probe card having a plurality of connection terminals for receiving from a tester a test signal and a power supply signal, said at least one probe card having a plurality of probe needles corresponding to said plurality of external pads, respectively;
simultaneously testing the semiconductor integrated circuits arranged in at least two columns to determine electrical characteristics of the semiconductor integrated circuits.	supplying said test signal and said power supply signal from said tester to said probe needles by way of said connection terminals in a completely independent manner; supplying said test signal and said power supply signal from said probe needles to said semiconductor integrated circuit chips, by way of said external pads, in a completely independent and concurrent manner; and measuring electric characteristics

of the semiconductor integrated circuit chips in a completely independent and concurrent manner.

The withdrawn claim merely required:

setting probe needles into contact with pads of semiconductor integrated circuits arranged in at least two columns.

The newly submitted reissue claim, on the other hand, requires:

preparing at least one semiconductor wafer, said semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in rows and columns, said semiconductor integrated circuit chips having a plurality of external pads; [and]

preparing at least one probe card, said probe card having a plurality of connection terminals for receiving from a tester a test signal and a power supply signal, said at least one probe card having a plurality of probe needles corresponding to said plurality of external pads, respectively.

With respect to testing the circuits, the withdrawn claim required only:

simultaneously testing the semiconductor integrated circuits arranged in at least two columns to determine electrical characteristics of the semiconductor integrated circuits.

Again, newly submitted claim 12 is much more specific, requiring all of:

supplying said test signal and said power supply signal from said tester to said probe needles by way of said connection terminals in a completely independent manner;

supplying said test signal and said power supply signal from said probe needles to said semiconductor integrated circuit chips, by way of said external pads, in a completely independent and concurrent manner; and

measuring electric characteristics of the semiconductor integrated circuit chips in a completely independent and concurrent manner.

Claim 12 as filed in the reissue application is thus narrower in all material respects in comparison with the claim that was withdrawn from the original application, and amended claim 12 is narrower still. The same is true of course of reissue claims 13-16, each of which depends from claim 12.

For these reasons, reissue claims 6-12 are not within the reach of the recapture doctrine, and the Examiner's withdrawal of those rejections is respectfully requested.

Claims 6-11 were rejected under section 112 as being allegedly "unclear how the recited steps are related to a method of manufacturing." [12]/ These claims have now been amended to recite "a method for testing semiconductor integrated circuits" in the preambles of the claims." This amendment is believed to overcome this rejection, and the rejection's withdrawal is thus respectfully requested.

Independent claims 6 and 12 were both rejected under section 102 as being allegedly anticipated by the Kwon patent. Those claim have both now been amended to require use of a "probe card [that] includes structure defining a rectangular through hole having first and second long sides" and "probe needles [that] extend through the rectangular through hole." Such a configuration is not present in the Kwon patent or any of the other references cited against the reissue application. Independent claims 6 and 12 are thus believed patentable over the cited art, and the allowance of those claims is therefore respectfully requested, along with claims 7-11 and 13-16, each of which depends in some way from one of these two independent claims.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at the Los

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[12]/ *Office Action*, ¶ 5.

Angeles, California telephone number (213) 337-6711 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: April 10, 2003

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Version with markings to show changes made:

6. (Amended) A method [of manufacturing integrated circuit chips,] for testing semiconductor integrated circuits, the method comprising:

providing a semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged [theron] thereon in two columns and at least two rows, each of said plurality of semiconductor integrated chips having a plurality of external terminals;

coupling a probe card to the semiconductor wafer through a plurality of probe needles on said probe card corresponding to said plurality of external terminals of each of said integrated circuit chips, said probe card receiving a plurality of independent test signals and a power supply signal from a tester, wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole;

concurrently supplying the independent test signals and the power supply signal from the tester through the probe needles to said plurality of external terminals of said plurality of integrated circuits; and

concurrently measuring electric characteristics of said semiconductor integrated circuit chips in an independent manner.

7. (Amended) The method [of manufacturing] of claim 6, wherein said external terminals are centrally disposed within said integrated circuit chips, with integrated circuits on either side of said external terminals.

8. (Amended) The method [of manufacturing] of claim 7, wherein said external terminals are arranged in a plurality of columns and rows.

9. (Amended) The method [of manufacturing] of claim 8, wherein the step of providing a semiconductor wafer [said providing] includes forming memory arrays for each of said integrated circuit chips.

10. (Amended) The method of [manufacturing according to] claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on internal layers of said probe card.

11. (Amended) The method of [manufacturing according to] claim 6, wherein the test signal and the power supply signal are supplied from said tester to said probe needles by way of a plurality of wiring lines on different internal layers of said probe card, said wiring lines positioned on different ones of said different internal layers according to a type of signal carried by said wiring lines.

12. (Amended) A probing test method of semiconductor integrated circuits, comprising:

preparing at least one semiconductor wafer, said semiconductor wafer having a plurality of semiconductor integrated circuit chips arranged thereon in rows and columns, said semiconductor integrated circuit chips having a plurality of external pads;

preparing at least one probe card, said probe card having a plurality of connection terminals for receiving from a tester a test signal and a power supply signal, said at least one probe card having a plurality of probe needles corresponding to said plurality of external pads, respectively, wherein said probe card includes structure defining a rectangular through hole having first and second long sides, and wherein the probe needles extend through the rectangular through hole;

supplying said test signal and said power supply signal from said tester to said probe needles by way of said connection terminals in a completely independent manner;

supplying said test signal and said power supply signal from said probe needles to said semiconductor integrated circuit chips, by way of said external pads, in a completely independent and concurrent manner; and

measuring electric characteristics of the semiconductor integrated circuit chips in a completely independent and concurrent manner.